WHAT IS CLAIMED IS:

1. A process for fabricating a low dielectric constant semiconductor comprising the steps of:

depositing a first metal layer on a substrate;

patterning said first metal layer to form a patterned first metal wiring;

forming a support structure on said patterned first metal wiring, wherein said support structure is a first insulating material has a dielectric constant K_1;

patterning said support structure;

depositing a second insulating material onto said support structure, wherein said second insulating material having a dielectric constant K_2;

planarizing said second insulating material;

depositing a polish-stop film layer over said planarized second insulating material;

forming a plurality of metal studs in said polish-stop film layer;

depositing a second metal layer onto said polish-stop film layer, to form a second metal wiring; and

patterning said second metal layer to form interconnects between said second metal wiring and said first metal wiring via said metal studs.

2. The process of claim 1, further comprising repeating each of said steps.

3. The process of claim 1, wherein said dielectric constant K_2 of said second insulating material is lower than said dielectric constant K_1 of said first insulating material.

4. The process according to claim 1, wherein said first metal layer is patterned by a process selected from the group comprising reactive ion etching or damascene.

5. The process of claim 1, wherein said support structure is formed by contact printing.

6. The process of claim 5, wherein said contact printing comprises the steps of:

forming a stamp,

forming a master connected to said stamp, wherein said master has a negative of a desired printing pattern,

curing said master and said stamp,

peeling said stamp away from said master, and

exposing said master to ink.

7. The process according to claim 1, wherein said step of depositing said second insulating material further comprising the steps of:

applying a non-porous material having a spacer; and

removing said spacer.

8. The process according to claim 7, wherein said removing step is carried out by heating.

9. The process of claim 1, wherein said planarizing step is carried out by a method selected from the group comprising etch back processing, chemical-mechanical polishing processing or any combinations thereof.

10. The process according to claim 9, wherein said etch back process comprises the steps of:

spin coating a material having the same etch rate as said second insulating material; and

etching said spin coated material to produce a planar surface on said second insulating material.

11. The process of claim 1, wherein said metal studs are formed by damascene process.

12. The process of claim 1, wherein said first insulating material is a low K dielectric having a dielectric constant less than 4.

13. The process of claim 1, wherein said first insulating material is a low K dielectric having a dielectric constant less than 3.

14. The process according to claim 1, wherein said first insulating material is selected from the group comprising polymers, organic polymeric materials, inorganic polymeric materials, polymeric resins, nonporous inorganic materials, organic-inorganic hybrid materials, low dielectric constant inorganic materials, low dielectric constant inorganic materials, or combinations thereof.

15. The process of claim 1, wherein said second insulating material is a low K dielectric with a dielectric constant less than 2.

16. The process of claim 1, wherein said second insulating material is a low K dielectric with a dielectric constant less than 1.8.

17. The process according to claim 1, wherein said second insulating material is a porous inorganic-organic hybrid.

18. The process according to claim 17, wherein said porous inorganic-organic hybrid is selected from the group comprising methylsilsesquioxane, porous hydridosilsesquioxane, porous methylsilsesquioxane-hydridosilsesquioxane copolymer, porous methylsilsesquioxane-hydridosilsesquioxane blends, porous tetraethylorthosilane, or any combinations thereof.

19. The process according to claim 1, wherein said second insulating material is a porous organic material.

20. The process according to claim 19, wherein said porous organic material is an aromatic thermosestting polymeric resin.

21. The process according to claim 1, wherein said first insulating material is non-porous.

22. The process according to claim 1, wherein said second insulating material is porous.

23. A low dielectric constant device prepared by a process comprising the steps of:

depositing a first metal layer on a substrate;

patterning said first metal layer to form a patterned first metal wiring;

forming a support structure on said patterned first metal wiring, wherein said support structure is a first insulating material having a dielectric constant K_1;

patterning said support structure;

depositing a second insulating material onto said support structure, wherein said second insulating material having a dielectric constant K_2;

planarizing said second insulating material;

depositing a polish-stop film layer over said planarized second insulating material;

forming a plurality of metal studs in said polish-stop film layer;

depositing a second metal layer onto said polish-stop film layer, to form a second metal wiring; and

patterning said second metal layer to form interconnects between said second metal wiring and said first metal wiring via said metal studs.

24. A process for fabricating a low dielectric constant semiconductor comprising the steps of:

depositing a first metal layer on a substrate;

patterning said first metal layer to produce a patterned first metal wiring;

forming a support structure on said patterned first metal wiring, wherein said support structure is a first insulating material having a dielectric constant K_1;

patterning said support structure;

depositing a second insulating material onto said support structure, wherein said second insulating material has a dielectric constant K_2 that is lower than said dielectric constant K_1 of said first insulating material;

planarizing said second insulating material;

depositing a polish-stop film layer over said planarized second insulating material;

forming a plurality of metal studs in said polish-stop film layer;

depositing a second metal layer onto said polish-stop film layer, thereby forming interconnects with said metal studs; and

patterning said metal layer to interconnect second metal wiring with first wiring via said metal studs.